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H4M
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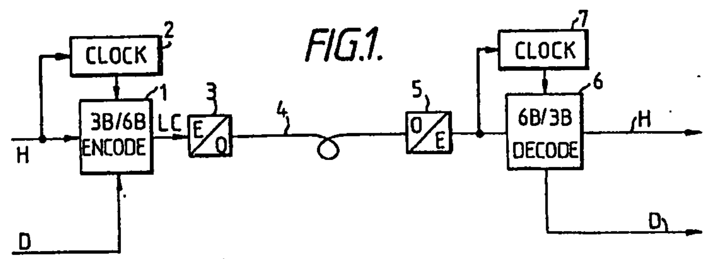
(54) Digital communication system

(57) To transmit an auxiliary data stream (D), e.g. service channel information, in an integrated manner together with a main data stream in a digital communication system, a block encoder (1) is provided on the send side, which converts the main data stream into a redundant block code having a word disparity of zero, in accordance with the logical status of the auxiliary data stream. Provided on the receive side is a block decoder (6) which performs block synchronisation on the basis of the word disparity of zero, derives the logical status of the auxiliary data stream (D) from the received code words of the block code, and converts the code words into the original main data stream again.

FIG.1.



The drawing(s) originally filed was (were) informal and the print here reproduced is taken from a later filed formal copy.

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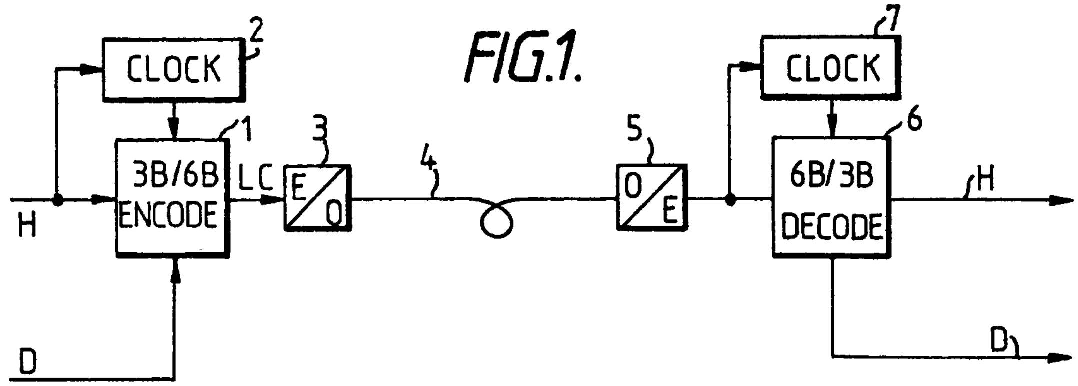


FIG.1.

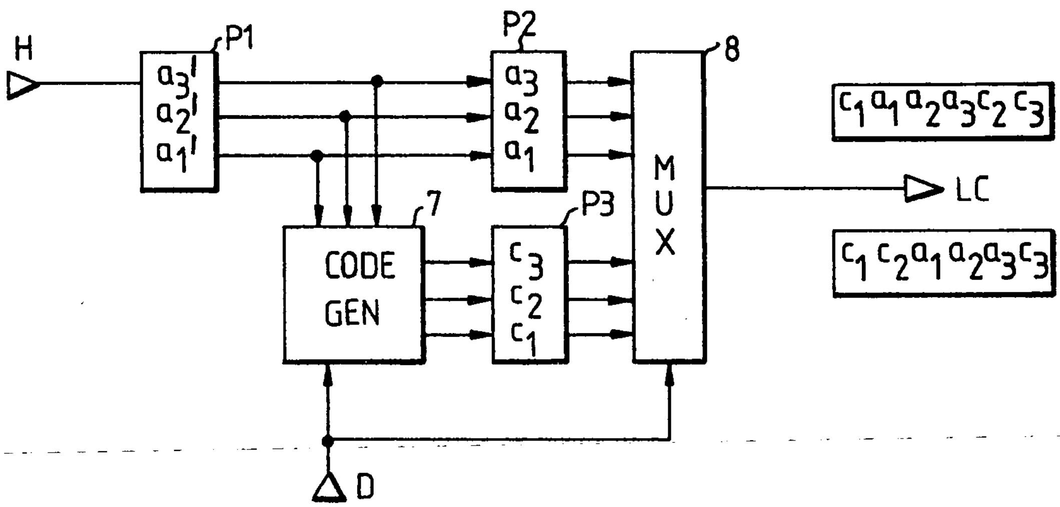


FIG.2.

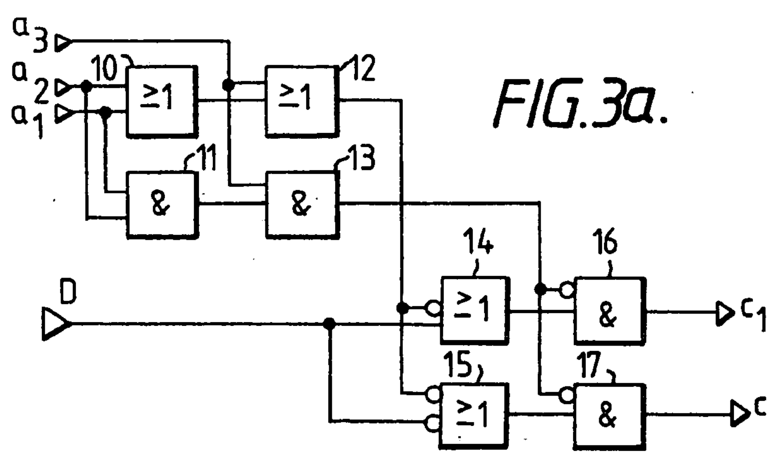


FIG.3a.

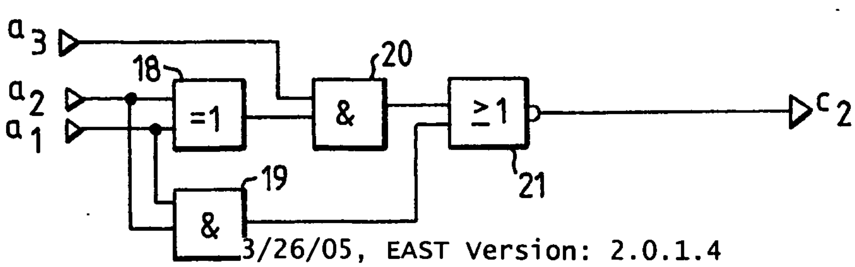


FIG.3b.

FIG.4.

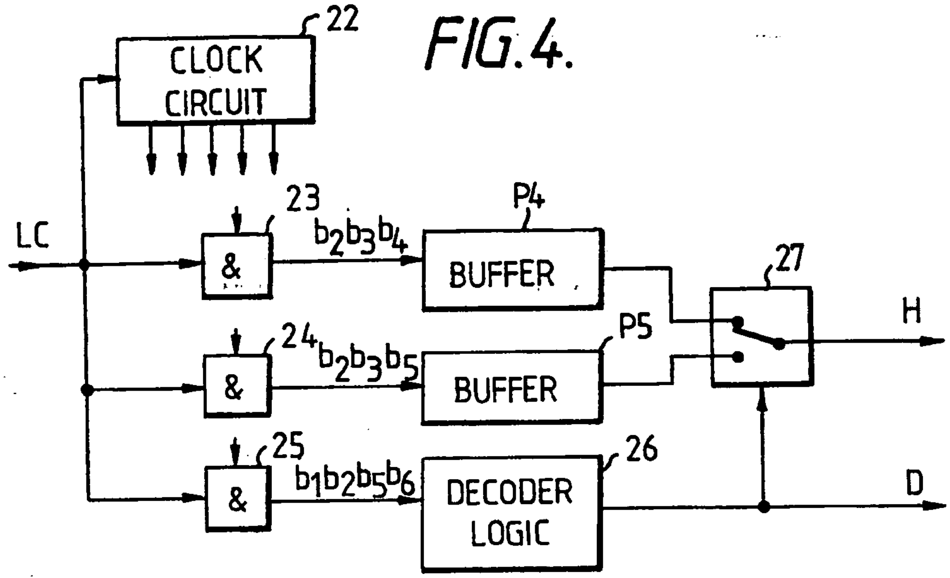


FIG.5.

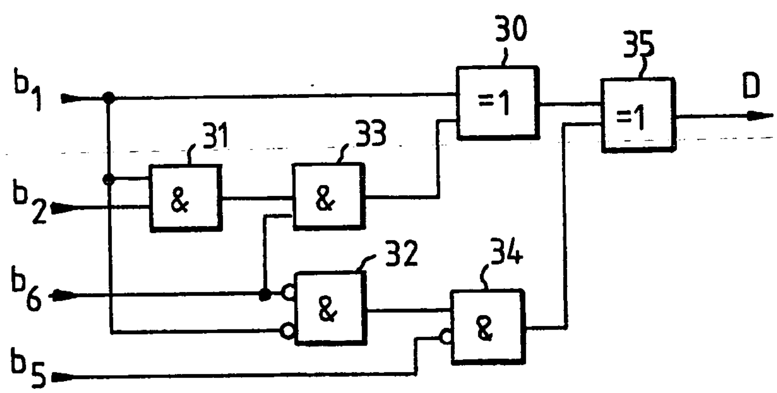
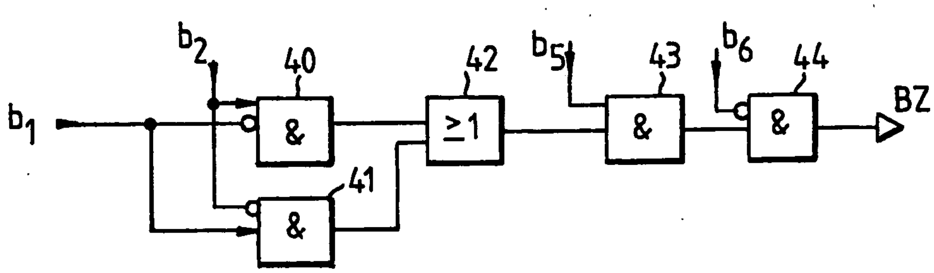


FIG.6.



SPECIFICATION

Digital communication system

The present invention relates to a digital communication system of the kind in which a main data stream and an auxiliary data stream having a lower bit rate are transmitted in an integrated manner.

A system of this kind is known from European Patent No. A10,059,395. In this system, the auxiliary data stream is transmitted by altering the power level as a function of the status of the auxiliary data stream. This system operates dependably when the bit rate of the main data stream is relatively high in comparison with the bit rate of the auxiliary data stream (e.g. 34 Mbit/s as opposed to 30 kbit/s). If the ratio between the bit rate of the main data stream and that of the auxiliary data stream is lower, i.e. if the main data stream is transmitted at a speed of 2 or 8 Mbit/s, for example, the degree of modulation is so high that the error frequency in the main data stream tends to increase excessively when the known system is employed.

It is therefore an object of the present invention to provide a communication system of the kind referred to ~~that~~ is suitable for relatively low main data stream bit rates.

According to the invention in its broadest aspect, a digital communication system of the kind referred to is characterised in that there is a block encoder on the send side, which divides the main data stream to be transmitted into sequential groups of n bits and converts them into a block code having m bits per word and a word disparity of zero, with m being greater than n, and with the selection of the code alphabet being controlled in such a manner that it is dependent upon the status of the auxiliary data stream, and in that there is a block decoder, on the receive side, which divides the received data stream into sequential m-bit words on the basis of the word disparity of zero, reconverts these m-bit words into the n-bit words and derives the logical status of the auxiliary data stream from the received data stream in accordance with the code alphabet from which they were taken.

In addition to the advantage of requiring only a minimal degree of circuitry sophistication, a system according to the invention offers the further advantage of employing a direct-current-free code. This eliminates the need for scrambling means, which would otherwise be necessary in order to ensure dependable receive-side timing recovery and prevent the optical senders from being subjected to excesssive loading.

An embodiment of the invention will now be defined by way of example with reference to the accompanying drawings in which:-

Figure 1 shows a block schematic diagram of the entire system,

Figure 2 shows a block schematic diagram of the send-side block encoder,

Figure 3a shows a logic diagram of a portion of the code generator according to Figure 2 for generating bits c_1, c_3,

Figure 3b shows a logic diagram of a portion of the code generator according to Figure 2 for generating bit c_2,

Figure 4 shows a block schematic diagram of the receive-side block decoder,

Figure 5 shows a schematic diagram of the decoder logic according to Figure 3, and

Figure 6 shows a logic diagram of the supplementary decoding circuit of the receive-side block decoder for recognition of the given operational status.

Shown on the send side in the system according to Figure 1 is a block encoder 1, which combines a main data stream H and an auxiliary data stream D into a transmission data stream, also called a line code LC. In doing so, block encoder 1 converts every n-bit group of main data stream H into a block code having m bits per word, in accordance with the status of auxiliary data stream D, with m being greater than n. Consequently, block encoder 1 is denoted a 3B/6B encoder, as it converts every three bits of the main data stream into a 6-bit code word, for example. Clock recovery means 2 are arranged for controlling the conversion in the timing of main data stream H. The data stream to be transmitted from the output of block encoder 1, denoted LC, is converted into an optical signal in an electrical-optical converter 3, which is transmitted via an optical transmission circuit 4 to an optical-electrical converter 5 on the receive side, where it is again separated into main data stream H and auxiliary data stream D in a block decoder 6, with further clock recovery means 7 being arranged for this purpose.

The rule under which block encoder 1 and block decoder 6 operate results from a code table for the block code being employed, for which 2 different examples are indicated below, which differ slightly from each other.

described below, when the clock is regenerated digitally its minimum jitter will be essentially equal to the period of the clock used by the regeneration state machine, added to all the other jitter sources in the system. That clock period should be minimized, and hence the clock frequency should be maximized.

Example 1:

3-bit group Main data stream	6-bit block code D = 0	D = 1
111	001110	011100
110	001101	111000
101	001011	110100
100	011001	110010
011	000111	101100
010	010101	101010
001	010011	100110
000	110001	100011
$a_1a_2a_3$	$c_1c_2a_1a_2a_3c_3$	$c_1a_1a_2a_3c_2c_3$

Example 2:

3-bit group Main data stream	6-bit block code D = 0	D = 1
111	001110	011100
110	001101	111000
101	001011	110100
100	011001	110010
011	000111	101100
010	010101	101001
001	010011	100101
000	110001	100011
$a_1a_2a_3$	$c_1c_2a_1a_2a_3c_3$	$c_1a_1a_2a_3c_2c_3$

The difference between the two code tables can be found in the next to the last and in the third from the last lines, where the two last bits in the right column, denoted c_2 and c_3, are 1 and 0 in Example 1 and 0 and 1 in Example 2. As can be seen from the code tables, a 3-bit group is converted into the 6-bit block code in accordance with the code alphabet at the left if the binary state of the auxiliary data stream is zero (D = 0) and in accordance with the code alphabet at the right if the binary state of the auxiliary data stream is 1 (D = 1). In all cases, the 3-bit group a_1, a_2, a_3 is included in the 6-bit code word without any alteration, with supplementary bits c_1, c_2 and c_3 being added to produce a 6-bit code word having a word disparity of zero.

The point at which the unaltered 3-bit group is inserted between supplementary bits c_1, c_2, c_3 differs. In the case of the code alphabet at the left (D = 0), insertion is between the second bit c_2 and the third bit c_3, while in the case of the code alphabet at the right, insertion is between the first bit c_1 and the second bit c_2 of the supplementary bits.

A block schematic diagram of a block encoder operating in accordance with either of Examples 1 or 2 will now be explained on the basis of Figure 2. In groups of 3 bits each, main data stream H is written into a buffer P1 serially and read out of it in parallel. From the outputs of buffer P1, each 3-bit group is provided to the inputs of a code generator 7 and to the inputs of a buffer P2, so that sequential 3-bit groups a_3', a_2', a_1', and a_3, a_2, a_1 are contained in buffers P1 and P2. Code generator 7 contains a simple logic circuit, which will be explained below on the basis of Figure 3; on the basis of 3-bit group a_1, a_2, a_3 and auxiliary data stream D, applied to another input, the logic circuit generates supplementary bits c_1, c_2, c_3, which, as already explained above, are added to each 3-bit group. Bits c_1, c_2, c_3 generated by code generator 7 are stored in a third buffer P3.

The bits stored in buffer P2 and buffer P3 are provided to parallel inputs of a multiplexer 8 which, controlled by auxiliary data stream D, inserts 3-bit group a_1, a_2, a_3 either between c_2 and c_3 (if D = O) or between c_1 and c_2 (if D = 1). This produces line code LC, which is suggested in Figure 2 at the output of multiplexer 8 and which is transmitted to the receiver over the transmission circuit.

That portion of the logic circuit required for generation of bits c_1 and c_3 will now be explained with reference to Figure 3a. Bits a_1 and a_2 are provided to the inputs of an OR circuit 10 and, simultaneously, to the inputs of an AND circuit 11; the output of OR circuit 10 is connected with an input of an OR circuit 12, and the output of AND circuit 11 with the input of a further AND circuit 13. Bit a_3 is provided to the other input of OR circuit 12 and AND circuit 13. The output of OR circuit 12 is connected to an inverted input of an OR circuit 14 and to an inverted input of an OR circuit 15. Auxiliary data stream D is supplied to a second input of OR circuit 14 and a second inverted input of OR circuit 15. The output of OR circuit 14 is connected to an input of an AND circuit 16, and the output of OR circuit 15 to an input of an AND circuit 17. The output signal of AND circuit 13 is provided to each of these AND circuits at an inverted input. Bit c_1 appears at the output of AND

circuit 16, while bit c_3 appears at the output of AND circuit 17.

As can easily be seen, the logic circuit according to Figure 3a generates bits c_1 and c_3 in accordance with the code table shown in Example 1 as a function of its input signals a_1, a_2, a_3 and D. A logic circuit operating in accordance with the code table shown in Example 2 would only need to be modified slightly in relation to that shown in Figure 3a.

Figure 3b shows that portion of the logic circuit of code generator 7 intended for generation of bit c_2. Bits a_1 and a_2 are provided simultaneously to inputs of an EXCLUSIVE-OR circuit 18 and inputs of an AND circuit 19. The output of EXCLUSIVE-OR circuit 18 is connected to an input of an AND circuit 20, to whose other input bit a_3 is supplied. The inputs of AND circuits 19 and 20 are connected to the inputs of a NOR circuit 21, whose output supplies bit c_2. As can easily be seen, this logic circuit supplies bit c_2 in accordance with the code table shown in Figure 1, whose two code alphabets are identical with respect to bit c_2 (second or fourth place). A logic circuit operating in accordance with the code table shown in Example 2 would only need to be modified slightly in relation to that shown in Figure 3b.

The receive-side block decoder will now be explained on the basis of Figures 4 to 6. Received line code LC is advanced from the optical-electrical converter (Figure 1) to a clock recovery circuit 22 and, simultaneously, to a plurality of AND circuits 23, 24 and 25. The clock recovery circuit provides block synchronisation and bit timing synchronisation on the basis of the line code received, with block synchronisation being based upon the block code having a word disparity of zero. Clock recovery circuit 22 also generates clock pulses for AND circuits 23 to 25, which cause each AND circuit to permit a certain combination of the bits contained in the code word to pass through it. In the case of the above-described 6-bit block code with bits b_1 to b_6, AND circuit 23 is controlled in such a manner that it permits bits b_2, b_3, b_4 of each 6-bit word to pass through it. Controlled in a corresponding manner, AND circuit 24 permits bits b_3, b_4, b_5 to pass through it and AND circuit 25, bits b_1, b_2, b_5, b_6. From the output of AND circuit 23, the bits that have been permitted to pass through it are supplied to a buffer P4, while the bits appearing at the output of AND circuit 24 are supplied to a buffer P5. A decoding logic circuit 26, for which a practical example is shown in Figure 5, derives the status of auxiliary data stream D from the output bits of AND circuit 25. Bits b_3, b_4 of each received 6-bit code word are not required for this purpose.

As can be seen from the two code tables, 3-bit group a_1, a_2, a_3 is located either in bit positions 2 to 4 or in bit positions 3 to 5 of the received code word; consequently, the bits of the main data stream are stored either in buffer P4 or buffer P5. Switching means 27 are provided for selec tion of one of these two possibilities, as a function of the status of auxiliary data stream D derived on the receive side; if D = 1, switching means 27 connects buffer P4 (and if D = 0, buffer P5) to the output of the block decoder, so that the sequential n/bit groups forming main data stream H appear at the output of switch 27.

The decoding logic according to Figure 5 for deriving the status of auxiliary data stream D from bits b_1, b_2, b_5 and b_6 is designed in the following manner: Bit b_1 is supplied to an input of an EXCLUSIVE-OR circuit 30, as well as to an input of an AND circuit 31 and to an inverted input of an AND circuit 32. Bit b_2 is supplied to the other input of AND circuit 31. Bit b_6 is supplied to a second inverted input of AND circuit 32 and to an input of an AND circuit 33, whose other input is connected to the output of AND circuit 31. The output of AND circuit 33 is connected to a second input of EXCLUSIVE-OR circuit 30. Bit b_5 is supplied to an inverted input of an AND circuit 34, whose other input is connected to the output of AND circuit 32. The outputs of AND circuit 34 and EXCLUSIVE-OR circuit 30 are connected to the inputs of an EXCLUSIVE-OR circuit 35, whose output supplies the status of auxiliary data stream D. It can easily be seen that this logic operation clearly produces the logical status of auxiliary data stream D, regardless of whether the decoding is performed in accordance with the code table shown in Example 1 or in accordance with the code table shown in Example 2.

The above-described encoding means that the transmitted data stream displays a bit rate that is increased in the ratio of m : n (2 : 1 in the example) relative to that of the main data stream. Since the invention is to be employed in conjunction with relatively low main data stream bit rates and on an optical transmission circuit, this increase does not pose any transmission problems due to the sufficient transmission capacity that is available.

Encoding in accordance with the indicated code tables offers very simple means for transmitting operational status information from the sender to the receiver. In accordance with a further development of the invention, the bits of the block-encoded data stream are inverted in the send-side block encoder if a given operational status of the sender exists, for example in the event of a defective amplifier, and only then transmitted. The receive-side block decoder is then provided with a supplementary decoding circuit, which recognises that the received data stream is the inverted block-encoded data stream and that the given operational status consequently exists. After identifying this fact, this supplementary decoding circuit then inverts the received data stream, thereby permitting it to be decoded in the above-described manner. Until this status is identified, the receive-side block decoder supplies an erroneous output signal; consequently, a portion of the information contained in the main data stream and the auxiliary data stream is lost. However this loss can be accepted, as a notification of this nature regarding a defective status of the sender could possibly prevent failure of the entire transmission circuit, i.e. a far greater loss.

To invert the block-encoded data stream in the send-side block encoder, it is merely necessary to provide it with an EXCLUSIVE-OR circuit, with the block-encoded data stream being provided to one of its inputs and a logical 1 signal being provided to its other input if the given operational status exists, whereby the EXCLUSIVE-OR circuit then puts out the block-encoded data stream with inverted polarity.

If the encoding is based upon the code table shown in Example 2, it is possible, by means of very simple circuitry, to recognise the inversion in the receive-side block decoder. Inversion of the block-encoded data stream is the same as an inverted code table which, on the basis of the normal code table in accordance with Example 2, would then look as follows:

3-bit group Main data stream	D = 0	6-bit block code D = 1
111	110001	100011
110	110010	000111
101	110100	001011
100	100110*	001101
011	111000	010011
010	101010*	010110*
001	101100	011010*
000	001110	011100

In this code table, those code words marked with an asterisk contain combinations of bits b_1, b_2, b_5, b_6 that are equal to 0110 or 1010. Such combinations of these bits do not occur in the normal code table in accordance with Example 2; consequently, their appearance in the code words of the received block code, if this occurs with sufficient frquency, serves as a dependable indication that the received data stream is the block-encoded data stream that has been transmitted in an inverted manner.

In this connection, the fact should also be mentioned that, because the word disparity is zero, the polarity inversion does not in any way impair block synchronisation in the receive-side block decoder.

A simple logic circuit in accordance with Figure 6 is suitable for identifying the above-mentioned bit combinations, which do not normally occur. This circuit is a decoding circuit provided additionally to that shown in Figure 5 and, similarly to it, is controlled by means of various bits of each code word. Bit b_1 is provided to an inverted input of an AND circuit 40, as well as to an univerted input of an AND circuit 41. Bit b_2 is provided to a further input of AND circuit 40 and to an inverted input of AND circuit 41. The outputs of both AND circuits 40 and 41 are connected to the inputs of an OR circuit 42, whose output is connected to one input of an AND circuit 43. Bit b_5 is supplied to its other input, and its output is connected to an input of an AND circuit 44, with bit b_6 being provided to its other, inverted input; its output supplies the logical status BZ, which represents reception of a bit combination that does not normally occur. As can easily be seen, output signal BZ has a logical status of 1 if bit combinations b_1, b_2, b_5, b_6 is either 0110 or 1010. To determine whether the given operational status is, in fact, present or whether there is a transmission error, it is then merely necessary to provide counting means, which determine whether the frequency of the occurrence of such bit combinations is higher than a threshold resulting from the statistical properties of the block code.

The fact should also be mentioned that the invention is by no means limited to the above-described 3B/6B block code. On the contrary all nB/mB block codes (where m is grater than n) which have a word disparity of zero and lend themselves to simple, yet reliable decoding are suitable. Moreover, it is also possible to convert a main data stream having more than 2 levels into a block code through the employment of more than 2 code alphabets.

CLAIMS

1. A digital communication system of the kind in which a main data stream (H) and an auxiliary data stream (D) having a low bit rate are transmitted in an integrated manner, characterised in that there is a block encoder on the send side, which divides the main data stream (H) to be transmitted into sequential groups of n bits (a_1, a_2, a_3) and converts them into a block code having m bits per word and a word disparity of zero, with m being greater than n, and with the selection of the code alphabet being controlled in such a manner that it is dependent upon the status of the auxiliary data stream (D), and in that there is a block decoder, on the receive side, which divides the received data stream (LC) into sequential m-bit words (b_1, b_2, b_3, b_4, b_5, b_6) on the basis of the word disparity of zero, reconverts these m-bits words into the n-bit words (a_1, a_2, a_3) and derives the logical status of the auxiliary data stream (D) from the received data stream in accordance with the code alphabet from which they were taken.

2. A system according to claim 1, characterised in that the block encoder performs this conversion of the n-bit groups into the block code with m bits per word, and in that the n bits occur in the m-bit word with unaltered binary values and in unaltered sequence (a_1, a_2, a_3).

3. A system according to claim 2, characterised in that the n bits assumed without alteration (a_1, a_2, a_3) are inserted in different positions between the other bits (c_1, c_2, c_3) of the m-bit word if different code alphabets are employed (c_1, c_2, a_1, a_2, a_3, c_3, or c_1, a_1, a_2, a_3, c_2, c_3).

4. A system according to claim 3, characterised in that the block encoder converts groups of three bits (a_1, a_2, a_3) of the main data stream to a 6-bit block code in accordance with the following table, as a function of the binary state of the auxiliary data stream (D):

3-bit group Main data stream	6-bit block code D = 0	D = 1
111	001110	011100
110	001101	111000
101	001011	110100
100	011001	110010
011	000111	101100
010	010101	101010
001	010011	100110
000	110001	100011
$a_1a_2a_3$	$c_1c_2a_1a_2a_3c_3$	$c_1a_1a_2a_3c_2c_3$

5. A system according to claim 3, characterised in that the block encoder converts groups of three bits (a_1, a_2, a_3) of the main data stream to a 6-bit block code in accordance with the following table, as a function of the binary state of the auxiliary data stream (D):

3-bit group Main data stream	6-bit block code D = 0	D = 1
111	001110	011100
110	001101	111000
101	001011	110100
100	011001	110010
011	000111	101100
010	010101	101001
001	010011	100101
000	110001	100011
$a_1a_2a_3$	$c_1c_2a_1a_2a_3c_3$	$c_1a_1a_2a_3c_2c_3$

6. A system according to claim 4 or 5, characterised in that the block decoder derives the status of the auxiliary data stream only from the bits of the m-bit word that are numbered 1, 2, 5 and 6.

7. A system according to any one of claims 1 to 6, characterised in that the send-side block encoder contains an inverting circuit, which inverts the block-encoded data stream as a function of the presence of a given operational status and in that the receive-side block decoder contains a further decoding circuit for recognition of the given operational status, as well as an inverting circuit, which inverts the received data stream prior to performance of the other decoding if the presence of the given operational status is recognised.

8. A system according to claim 7, characterised in that the further decoding circuit checks whether there are 6-bit words in the received data stream whose bits (b_1, b_2, b_5, b_6) that are numbered 1, 2, 5, 6 are equal to 0110 or 1010 in this sequence.

9. A digital communication system substantially as described with reference to the accompanying drawings.

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